Docket No.:   2003P12591

# CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of PCT/EP2005/050050, filed with the European Patent Office on January 7, 2005.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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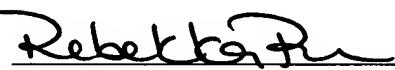
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1   Description

2

3   Device and method for equalizing the charge of serially

4   connected capacitors belonging to a double layer capacitor

5

6   The invention relates to a device for equalizing the charge

7   of the serially connected capacitors belonging to a double

8   layer capacitor, particularly in a motor vehicle electrical

9   system, according to Claim 1 or 2.

10

11  The invention also relates to a method for operating this

12  device according to Claim 5.

13

14  Double layer capacitors have proved to be the most favorable

15  technical solution for the storage and delivery of short-term

16  high power levels in a motor vehicle electrical system, for

17  example with regard to acceleration support (boosting) for

18  the internal combustion engine by means of an integrated

19  starter/generator functioning as an electric motor or to the

20  conversion of kinetic energy into electrical energy during

21  the regenerative braking process (recuperation) by means of

22  an integrated starter/generator functioning as a generator.

23

24  The maximum voltage of a single capacitor of a double layer

25  capacitor is limited to about 2.5V to 3.0V, with the result

26  that for a voltage of for example 60V – a typical voltage

27  value for a double layer capacitor used in a 42V vehicle

28  electrical system – about 20 to 25 single capacitors need to

29  be serially connected to form a capacitor stack.

30

31  Dependent on the differences in the spontaneous discharge of

32  the single capacitors (in the region of about 5% to 8% within

33  16 hours), a charge imbalance builds up in the capacitor

1  stack over the course of time which ultimately renders the
2  double layer capacitor unusable unless a charge equalization
3  is performed. If the discharge curve is extrapolated to
4  periods of weeks and months, which are relevant in the case
5  of motor vehicles, then the existing problem becomes obvious.
6
7  It is not however possible to perform a simple charge
8  equalization for a double layer capacitor, for example by
9  slightly overcharging the stack as in the case of a lead-acid
10 accumulator.
11
12 With regard to a large number of serially connected
13 accumulators, a method is known from EP 0 432 639 B2 for
14 performing a charge equalization between a weakly charged
15 accumulator and the group of remaining accumulators by
16 providing for each individual accumulator in the accumulator
17 stack a comparator circuit and a charging circuit, which
18 includes a squarewave function generator, and also a diode, a
19 transformer and a contact breaker. By means of this device
20 functioning as a flyback converter (using the isolating
21 transformer principle), energy is removed from the entire
22 stack and this is subsequently fed back into the most
23 discharged accumulator.
24
25 This effort may be justified for two or three accumulators,
26 but it is decidedly too high for a stack comprising twenty or
27 more accumulators/capacitors.
28
29 The object of the invention is to create a device having a
30 simplified structure which can be used to achieve self-
31 controlled operation for charge equalization between the
32 single capacitors in the capacitor stack of a double layer
33 capacitor with limited engineering effort. The object of the

1   invention is also to specify a method for operating this

2   device which enables functional monitoring of the device and

3   of the capacitor stack to be performed.

4

5   This object is achieved according to the invention by a

6   device according to the features described in Claim 1 or 2

7   and a method according to the features described in Claim 5.

8

9   Advantageous developments of the invention are set down in

10  the subclaims.

11

12  Embodiments according to the invention will be described in

13  detail in the following with reference to a schematic

14  drawing. In the drawings:

15

16  Figure 1   shows the circuit of a first embodiment according

17             to the invention,

18  Figure 2   shows voltage waveforms for selected points of this

19             circuit,

20  Figure 3   shows current waveforms for selected points of this

21             circuit,

22  Figure 4   shows the circuit of a second embodiment of the

23             invention.

24

25  Figure 1 shows the circuit of a first embodiment according to

26  the invention with a double layer capacitor DLC having one

27  positive and one negative terminal V+ and V-, and consisting

28  of n serially connected single capacitors C1 to Cn.

29

30  The circuit has a flyback transformer Tr0 whose primary and

31  secondary windings are wound in phase opposition to one

32  another and which has the function of a magnetic energy

33  store. The spots drawn in for the transformers in Figures 1

1  and 4 denote the respective start of the winding.

2

3  The primary winding of the flyback transformers Tr0 is

4  connected on the one hand to the positive terminal V+ and on

5  the other hand to the drain terminal of a switching

6  transistor T1 taking the form for example of a MOSFET. The

7  switching transistor T1 can however also take the form of a

8  bipolar transistor with base, emitter and collector

9  terminals. The source terminal of the switching transistor T1

10  is connected on the one hand to the inverting input of a

11  first voltage comparator KOMP1 and on the other hand by way

12  of a first resistor R1 to the negative terminal V- which is

13  at the reference potential (ground) of the circuit.

14

15  The gate terminal of the switching transistor T1 is connected

16  to the output of a first AND element UND1, to whose one input

17  a control signal EN which is supplied by an external control

18  logic circuit that is not shown is fed, and whose other input

19  is connected to the output of a second AND element UND2.

20

21  The noninverting input of the first voltage comparator KOMP1

22  is connected to a single-ended reference voltage Vref1 and

23  its output is connected to an input of the second AND element

24  UND2 and to a first input of a monitoring unit DIAG

25  (diagnosis).

26

27  One terminal of the secondary winding of the flyback

28  transformer Tr0 is connected directly, the other terminal by

29  way of a first diode D0 and a second resistor R2, to the

30  negative terminal V-. A first capacitor C0 is connected on

31  the one hand to the cathode of the first diode D0 and on the

32  other hand to the negative terminal V-. The connection point

33  of the cathode of the first diode D0 and the second resistor

1  R2 is connected to the inverting input of a second voltage

2  comparator KOMP2, whereas the reference voltage Vref1 is

3  applied to the latter's noninverting input.

4

5  The output of the second voltage comparator KOMP2 is

6  connected on the one hand to the other input of the second

7  AND element UND2 and on the other hand to a second input of

8  the monitoring unit DIAG.

9

10 A third input of the monitoring unit DIAG is connected to the

11 inverting input of the second voltage comparator KOMP2 and a

12 second single-ended reference voltage Vref2 is applied to a

13 fourth input of the monitoring unit DIAG. The output of the

14 monitoring unit DIAG delivers a status signal ST which is

15 monitored by an external evaluation logic circuit, not shown,

16 which will be described in detail later.

17

18 Each single capacitor C1 to Cn of the double layer capacitor

19 DLC is assigned a single transformer Tr1 to Trn which is

20 wound in-phase (primary and secondary windings are wound in-

21 phase with respect to one another).

22

23 The start of winding of the secondary winding of each single

24 transformer Tr1 to Trn is connected by way of a single diode

25 D1 to Dn to the positive terminal +C1 to +Cn of the single

26 capacitor C1 to Cn associated with it, while the other

27 terminal is connected directly to the other (negative)

28 terminal of the single capacitor C1 to Cn associated with it.

29

30 The primary windings of the single transformers Tr1 to Trn

31 are connected in parallel, whereby the common start of

32 winding is connected to the cathode of the first diode D0 and

33 the common end of winding is connected to negative terminal

1 V- (reference potential) and to the end of winding of the

2 secondary winding of the flyback transformer Tr0. In this

3 situation, the connection between the flyback transformer

4 (Tr0) and the single transformers is implemented by means of

5 a two-wire bus cable.

6

7 The method for operating this device is described in the

8 following with reference to signal waveforms illustrated in

9 Figures 2a to 2e (voltages) and also 3a and 3b (currents) for

10 selected points of the circuit. It is assumed in this

11 situation that the nominal voltage of the double layer

12 capacitor DLC = 10V, and the nominal voltage of a single

13 capacitor = 2.5V, where n = 4. A charge equalization takes

14 place here from the overall voltage of the double layer

15 capacitor DLC, but can also take place from other energy

16 storage devices as soon as any such are connected to the

17 double layer capacitor DLC, which is not however shown in

18 Figure 1.

19

20 By means of the aforementioned control signal EN (Figure 2a,

21 start at point in time t = 1µs), for the duration of the

22 latter the switching transistor T1 is released by way of the

23 AND element UND1 (Figure 2b shows the voltage at the drain

24 terminal of the switching transistor T1; up to point in time

25 t = 1µs the voltage at the drain terminal is +10V, at point

26 in time t = 1µs it drops to approximately 0V). If the control

27 signal EN and the output of the AND element UND2 are High

28 level, then switching transistor T1 is made conducting

29 (Figure 2e, t = 1µs).

30

31 A current begins to flow from the positive terminal V+

32 through the primary winding of the flyback transformers Tr0,

33 through the switching transistor T1 and the first resistor R1

1   to the negative terminal V- (Figure 3a), whereby a voltage

2   proportional to this current is present at the first resistor

3   R1 (Figure 2c).

4

5   The voltage present at the first resistor R1 rises as the

6   current flow increases, in other words also as charging of

7   the core of the flyback transformer Tr0 increases. If it

8   reaches the value of the reference voltage Vref1 at point in

9   time $t \cong 2.2\mu s$, then the voltage comparator KOMP1 switches

10   its output from High to Low level, whereupon the output of

11   the AND element UND" likewise goes to Low level and thus

12   makes the switching transistor nonconducting. The voltage

13   comparator KOMP1 is thus used for sensing the primary current

14   of the flyback transformer Tr0.

15

16   Since the current flowing through the first resistor R1 now

17   drops rapidly, the voltage present at it is also reduced and

18   drops below the value of the reference voltage Vref1. The

19   output from KOMP1 would now immediately return to High level,

20   as a result of which switching transistor T1 would again be

21   made conducting.

22

23   In order to prevent this, the voltage jump occurring on the

24   secondary side when switching off the flyback transformer Tr0

25   is detected and used in order to keep switching transistor T1

26   nonconducting until the flyback transformer Tr0 has been

27   completely discharged.

28

29   When the switching transistor T1 is made nonconducting, the

30   voltage of the primary side of the flyback transformer Tr0

31   rises - driven by the energy stored in its core - beyond the

32   voltage at the positive terminal V+. The voltage at its

33   secondary side rises likewise; the current caused by it flows

1  by way of the first diode D0 operated in the forward
2  direction (Figure 2d) and at the second resistor R2 generates
3  a proportional voltage whose rate of rise is determined by
4  the charging of the first capacitor C0. This voltage reaches
5  the inverting input of the voltage comparator KOMP2. The
6  latter is thus used for sensing the secondary voltage of the
7  flyback transformer Tr0.
8
9  As long as this voltage is greater than the reference voltage
10  Vref1, the output from the voltage comparator KOMP2 switches
11  to Low level, such that switching transistor T1 remains
12  nonconducting by way of the AND elements UND2 and UND1. Only
13  when the flyback transformer Tr0 is completely discharged and
14  the voltage breaks down on its secondary side does the
15  voltage at the inverting input of the voltage comparator
16  KOMP2 drop below the reference voltage Vref1, whereupon its
17  output goes to High level and makes the switching transistor
18  T1 conducting again by way of the AND elements UND2 and UND1.
19
20  The fact that the voltage at the secondary winding of the
21  flyback transformer Tr0 becomes negative when the switching
22  transistor T1 is made conducting is unimportant in this
23  situation because the first diode D0 is now blocking.
24
25  After the switching transistor T1 is made nonconducting, the
26  energy stored in the flyback transformer Tr0 flows by way of
27  the secondary winding of the flyback transformer Tr0 and the
28  first diode D0 to the first capacitor C0 and to the parallel-
29  connected primary windings of the small single transformers
30  Tr1 to Trn and thence by way of their secondary windings and
31  also the single diodes D1 to Dn to the single capacitors C1
32  to Cn.
33

1   The rapid current rise in the secondary winding of the
2   flyback transformer Tr0 associated with making the switching
3   transistor T1 nonconducting initially charges the first
4   capacitor C0. By this means, the magnetizing inductances of
5   the single transformers Tr1 to Trn receive sufficient time to
6   build up current such that a current can ultimately also flow
7   on their secondary sides.
8
9   On the secondary side of a single transformer, Tr1 for
10  example, a voltage is thus produced which corresponds to the
11  sum of the charging voltage of the single capacitor C1 and
12  the forward voltage of the single diode D1. This is also the
13  case in the same manner for the secondary voltages of the
14  transformers Tr2 to Trn. A typical value for this voltage is
15  for example 3.2V, whereby the charging voltage of C1 is 2.5V
16  and the forward voltage of D1 is 0.7V. When Schottky diodes
17  are used, the diode forward voltage is only about 0.3V.
18
19  The primary voltage of each single transformer is given by
20  the respective secondary voltage and the transformation ratio
21  - which is set to be identical for each single transformer
22  Tr1 to Trn.
23
24  It follows from this that different primary voltages for the
25  transformers Tr1 to Trn also result for different charging
26  voltages of the single capacitors C1 to Cn.
27
28  However, since the primary windings of all the transformers
29  Tr1 to Trn are now connected in parallel, this necessarily
30  results in a uniform primary voltage - and thus also a
31  uniform secondary voltage.
32
33  In this situation, this uniform primary voltage is caused by

1 the single capacitor, C1 for example, having the lowest

2 charging voltage because the latter actually also produces

3 the lowest primary voltage at the single transformer Tr1

4 assigned to it.

5

6 This uniform primary voltage is also present - transformed

7 with the reciprocal transformation ratio of the transformers

8 - at the secondary sides of all the other transformers Tr2 to

9 Trn.

10

11 However, since this voltage is now lower than the sum of the

12 charging voltage of the respective single capacitor C2 to Cn

13 and the forward voltage of the assigned single diode, these

14 single diodes D2 to Dn will not conduct and the single

15 capacitors C2 to Cn receive no charging current. Rather, the

16 current coming from the secondary side of the flyback

17 transformer Tr0 essentially flows to the single capacitor

18 (C1) with the lowest voltage as a charging current.

19

20 During the course of the charging process the voltage of this

21 capacitor will now rise and it reaches the value of the

22 capacitor with the second lowest voltage. From this point on

23 the single diode assigned to this capacitor also becomes

24 conducting and this capacitor too receives a part of the

25 charging current. Therefore, from this point on the voltages

26 of both capacitors will rise until their voltage reaches the

27 value of the capacitor with the third lowest voltage, etc.

28

29 This process is repeated until all the capacitors C1 to Cn in

30 the stack ultimately have the same voltage. With that, the

31 charging process is then completed.

32

33 By means of the monitoring circuit DIAG, the signal duration

1 = charging time which can be measured at the output of the
2 voltage comparator KOMP1 and the signal duration =
3 discharging time for the flyback transformer Tr0 which can be
4 measured at the output of the voltage comparator KOMP2 are
5 measured and compared with predefined upper and lower limit
6 values.
7
8 If the measured times lie within the predefined limit values,
9 then it can be assumed that the double layer capacitor DLC
10 and the charge equalizing circuit are in a perfect state.
11 Faults such as a short circuit or open circuit in individual
12 single capacitors can be easily detected in this manner.
13
14 An additional measurement of the rectified secondary voltage
15 of the flyback transformer Tr0 (Figure 2d) furthermore
16 permits detection of the lowest voltage of a single capacitor
17 C1 to Cn by, for example, capturing the amplitude in the
18 timing dimensions according to Figure 2d, approximately 0.2µs
19 to 1.0µs after the rise in the voltage and the transient
20 reaction. This value is proportional to the currently
21 smallest voltage of a single capacitor.
22
23 A comparison of this value with predefined upper and lower
24 limit values likewise provides information about the
25 operation of the double layer capacitor DLC.
26
27 The overall status of the double layer capacitor DLC captured
28 in this manner is displayed on the output of the monitoring
29 unit DIAG by means of a status signal ST with the
30 corresponding level. This status signal ST indicates whether
31 the double layer capacitor DLC is functioning fault-free or
32 whether a visit to a workshop is required for investigation
33 or repair.

1

2 Figure 4 shows the circuit for a second embodiment according

3 to the invention, which is essentially identical to the

4 circuit according to Figure 1, apart from the fact that in it

5 the flyback transformer Tr0 is replaced by an inductor L1 and

6 a transistor T2, for example a PNP transistor, and a third

7 resistor R3, are additionally added.

8

9 At the point at which the flyback transformer Tr0 was to be

10 found in Figure 1, the circuit includes an inductor L1. The

11 one terminal of the inductor L1 is connected to the positive

12 terminal V+ and the other terminal is connected on the one

13 hand to the drain terminal of the switching transistor T1 and

14 on the other hand by way of a first diode D0 and a third

15 resistor R3 to the emitter terminal of a transistor T2

16 operated as a level converter, whose base terminal is

17 connected to the positive terminal V+ and whose collector

18 terminal is connected to the second resistor R2 and the

19 inverting input of the voltage comparator KOMP2. The first

20 capacitor C0 is connected on the one hand to the cathode

21 terminal of the first diode D0 and on the other hand to the

22 positive terminal V+.

23

24 The connection between the primary windings of the single

25 transformers Tr1 to Trn and the inductor L1 is implemented

26 such that the interconnected starts of windings are connected

27 to the connection point of first diode D0 and third resistor

28 R3, and that the interconnected ends of windings are

29 connected to the positive terminal V+.

30

31 The remainder of the circuit is, as already mentioned,

32 identical to that according to Figure 1. With regard to this

33 embodiment too, the connection between the inductor (L1) and

1   the single transformers is implemented by means of a two-wire
2   bus cable.
3
4   With regard to this circuit, the measurement of the
5   discharging voltage of the inductor L1 must be related to the
6   voltage present at the positive terminal V+, which is done by
7   means of the PNP transistor T2 operated as a level converter.
8
9   If switching transistor T1 has been made conducting and its
10  drain voltage is therefore low, then the first diode D0 is
11  blocking and thus prevents a current from flowing from the
12  inductor L1 through the base/emitter diode of transistor T2
13  in the inverse direction.
14
15  Since the base voltage of transistor T2, which is at the
16  potential of the positive terminal V+, is now higher than its
17  emitter voltage, transistor T2 is turned off and the voltage
18  at R2 or at the inverting input of the voltage comparator
19  KOMP2 is 0 volts.
20
21  If the voltage at the inductor L1 jumps above the potential
22  at the positive terminal V+ after the switching transistor T1
23  has become nonconducting, then the first diode D0 is made
24  conducting and a current begins to flow from the inductor L1
25  by way of the first diode D0, the third resistor R3,
26  transistor T2 and the second resistor R2 to the negative
27  terminal V- (reference potential).
28
29  At the second resistor R2 this current generates a positive
30  voltage which, as described in the case of the embodiment
31  according to Figure 1, is higher than the reference voltage
32  Vref1, with the result that the output from the voltage
33  comparator KOMP2 switches to Low level, which ultimately

1   makes switching transistor T1 nonconducting, by way of the

2   AND elements UND2 and UND1.

3

4   Only when the inductor L1 is completely discharged does its

5   discharging voltage drop to almost reference potential,

6   whereupon the current flow through the second resistor R2

7   breaks down and switching transistor T1, as described in the

8   case of the embodiment according to Figure 1, is made

9   conducting again.

10

11  The remainder of the mode of functioning of the circuit and

12  the method for operating the circuit are identical to the

13  case of the embodiment according to Figure 1, as already

14  described further above.

15

16